Motor Hardware-in-the-loop System (HiL)

Cutting edge tool for Motor Controller development

A&D
Discover Precision

FPGA Board to run Motor Models at high speeds

- Supports wide range of development process including Motor Control Unit development and verification.
- Interface board equipped with the industry's largest FPGA
  - Xilinx Kintex-UltraScale, Large RAM, 200MHz sampling rate
  - Equipped with high-speed analog/digital interface.
  - supports multiple motor simulations and precise modeling
  - Installed on A&D HiLS dedicated platform "HELIOS"
  - Motor models can be run as fast a 1-2μsec time step

Ready to use application

- Supports Simulink Models
- FPGA code can be generated using either Xilinx System Generator or HDL Coder
- User can choose appropriate motor model according to application, from precision models such as JMAG-RT motor model, PMSM spatial harmonic model or PMSM LdLq motor model.
- Standard application
  - Simulink models for PMSM motor LdLq model, inverter model, sensor model, motor load model, motor controller model, GUI
- A&D also supports engineering such as harness manufacturing, model customization, automated test systems and training.

Features

- Turnkey solution
- Multiple Platforms
  - HELIOS-PRO/HELIOS-LITE
  - CPU: Xeon(4core)/core i3(2core)
  - VS2000-010-060/115
- VB power supply (600W)
- Equipped with Interface for MCU connection
- Failure Simulation circuits, load emulation

Motor Model

| PMSM LdLq Model |
| PMSM Spatial Harmonic Model JMAG |

Inverter Model

Ideal SW type	Failure simulation
	·Open/Short Gates
Ron/Roff emulation (snubber)	·U/V/W disconnect/short
	·Diode failure
	Loss calculation

Other Models

| Motor Controller Model |
| Voltage Boost Model |

Sensor Model

Resolver	Failure simulation
	·Sensor failure
Encoder	
Current sensor	

Motor HILS UserFPGA Model
Motor HILS CPU Model
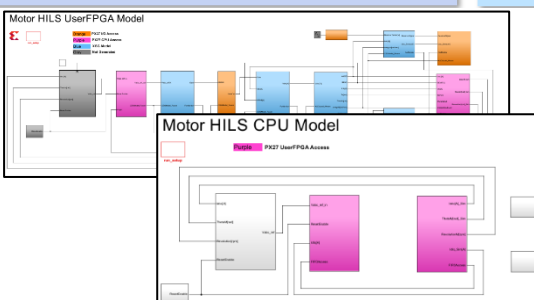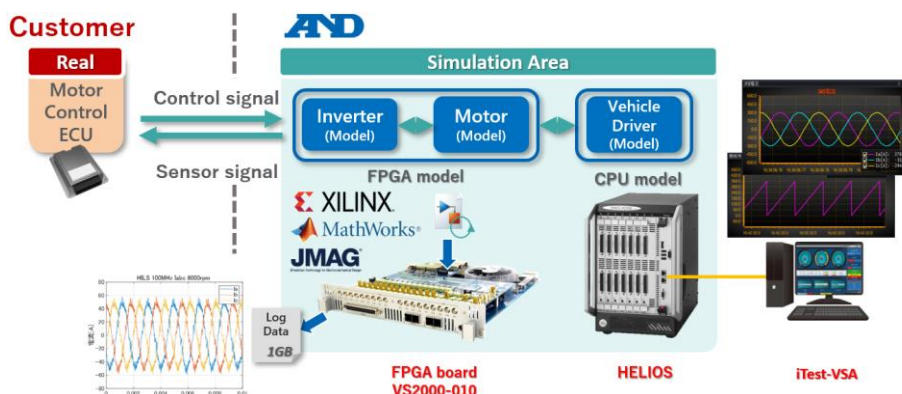
Application example

- Verification of power train Motor Control Unit for HEV/EV
- Plant model development

Features

- High speed data logging
- Efficient plant model development
- Failure simulation
- Model and electrical failures
- Self-diagnosis

Interface

- High-speed I/O interface
- Up to 200MHz sampling
- High-speed communication
  between FPGAs

Variety of debugging functions

- DRAM enables signal logging on FPGA up to 100Msps
- Simulation of model failures, open and short circuit, disconnection failures
- Equipped with self-diagnostic function. Makes it is easy to perform daily inspection and identify problems.

Board specifications

New high-end VS2000-010-060/115 FPGA board.
Ideal for high-speed and large-scale simulation.

Spec		AD5440-PX27	VS2000-010-060	VS2000-010-115
FPGA	FPGA	Kintex7 (XC7K410T)	Kintex UltraScale (KU060)	Kintex UltraScale (KU115)
	FPGA Logic Cell	306k	725k	1451k
	DSP	1540	2,760	5,520
	RAM	28.6Mb	38Mb	75.9Mb
I/O	AI	6+6ch/12.5MHz/14bit	4ch/100MHz/16bit	
	AO	6+6ch/12.5MHz/14bit	14ch/50MHz/14bit	
	DI	LVTTL: 16ch/25MHz RS422: in 10ch, out 6ch/32MHz LVDS : in 20ch, out 20ch/125MHz	12ch/200MHz	
	DO		4ch/200MHz	
Sampling Frequency		125 MHz	200 MHz	
FPGA communication		×	8 lane ×2 port 5Gbps (Aurora IP)	
Fail relay		× (External IF BOX)	○	
FPGA development environment		AD5440-PX27 Blockset (XSG) Matlab R2016b Vivado 2017.3	VS2000-010 Blockset (XSG / HDL coder) Matlab R2019b Vivado 2020.2	